IC Design:

Concept to Product

Training Programme

by

Faculty of Engineering

Multimedia University

Overview

This course covers the Integrated Circuits (IC) design cycle from the concept of designing, manufacturing and testing ICs with brief introduction to Application Specific Integrated Circuit (ASIC). This course will provide a comprehensive knowledge in circuit design, multiple techniques used and its advantages during circuit implementation. Emphasis will be given on practical knowledge to ensure participants are able to translate their knowledge obtained here to the real-world circuit design.

Objective

Upon completion of this course, participants are able to:

- Understand the integrated circuits (IC) design flow in CMOS technology.
- Describe some advanced knowledge in digital design techniques and methodologies.
- Apply the knowledge learnt with practical use of electronic design automation (EDA) tools.

Target Audience

The course is suitable for electronic engineering students and engineers who are interested in pursuing their career path in IC design.

Prerequisite

Basic knowledge in digital electronics.

Training Methodology

This course will have a ratio of approximately 60% lecture and 40% practical. Participants will build modules in accordance with the IC design flow in order to build better understanding of the course.This course can be conducted in virtual classroom mode.

Course Duration

2 days with 4 hours/day.

Content/Outline

Day 1:

Introduction to IC and ASICs design flow:

- IC Design Methodology
- Standard cell based ASIC
- Semi-custom ASIC and full custom ASIC
- Generic technology aspects and trends

Design library:

- Definition of library architecture (basic introduction to IOs, Memories, IPs, etc)
- Library characterization (standard load, parasitic caps, delay calculation, etc)
- Trends in Library characterization in terms of power, speed optimization, area).

Logic simulation and synthesis:

- Simulation modes (behavioural, functional, static timing analysis, gate level simulation)
- Cell model and testbenches
- Limitations in logic simulation
- Introduction to static timing analysis (STA)

Day 2:

Logic synthesis:

- Logic synthesis in the IC design flow.
- HDL and synthesis – some HDL guidelines
- Constraints and operating conditions
- Timing driven synthesis

Floorplan, Placement & Routing, Verification & DFM:

- Basics on floorplan (Hierarchical design, I/O and power planning, clock planning).
- Placement and routing, back-annotation, circuit extraction
- Need for verification
- Need for DFM and yield optimization

Current trends in the IC/ASIC arena:

- Some examples of the current trends in the IC/ASIC arena.

Course Instructor

Name: Ir. Dr. Lee Lini

Lini Lee received her B. Engg., M. Sc and Ph.D. degrees from Universiti Putra Malaysia, Malaysia in 1999, 2001 and 2008 respectively. She joined the industry working on supporting Synopsys EDA tools in 2001. Then, she came back to university to pursue her Ph.D. In 2008, she joined Freescale working as a Staff Engineer.

In 2010, she left the industry to join Multimedia University (MMU) and since then, she has been with Faculty of Engineering, MMU where she's currently a Senior Lecturer. Her main areas of research interest are integrated circuit (IC) design in both digital and analog, especially at low power applications. Dr Lini is an active Senior Member of IEEE CAS Malaysia Chapter, a Professional Engineer (PEng) with Board of Engineer Malaysia (BEM) and a Chartered Engineer (CEng) with the Institution of Engineering and Technology (IET).

Administrative Details

Programme Logistics

Duration: 2 days

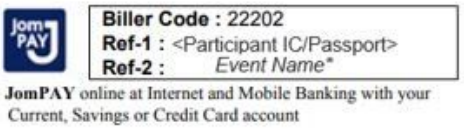
Dates, registration deadline and registration form:

Please refer to: https://www.mmu.edu.my/foe/short-courses/

Your Investment

Condition		Price per Pax
Regular Fee	Students / MMU Alumni	RM500
	Public	RM800
	Public (Group >5 pax)	RM600
	IEEE/IEM Members	RM700
Early Bird Fee	Students / MMU Alumni	RM300
	Public	RM600
	Public (Group >5 pax)	N/A
	IEEE/IEM Members	RM500

Method of Payment

<table>
<tr><th>Type of Payment</th><th>Method</th><th>Details</th></tr>
<tr><td rowspan="2">Local Transaction / Payment within Malaysia</td><td>Online Payment with JomPay</td><td>
• To get started, login to any preferred internet banking.
• Look for JomPay to begin the payment process.
• Enter Ref 1 & Ref 2.


JomPAY online at Internet and Mobile Banking with your Current, Savings or Credit Card account

* Ref. 2: FOEICDesign
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• To get started, go to MMU website (https://www.mmu.edu.my/) > Admission > Financial Info > Payment Channel > Non Student ;


or scan the QR code below to begin the process:


• Choose Category: Public Training
• Workshop Name
• Choose Your Participant Type:
✓ STUDEN (MMU, IEEE, IEM, Other Higher Learning Institution)
✓ PUBLIC
✓ GROUP (Group > 5 Pax)
✓ IEEE/M (IEEE/IEM Members)
</td></tr>
</table>

Type of Payment	Method	Details
International Payment / Payment outside Malaysia	Online payment with Flywire	• To get started, go to mmulanding.flywire.com; or scan the QR code to begin the payment process: SCAN ME • Choose Conference for Non-students related

Note:

Please submit the proof of payment to organizer for clearance updating purposes within 2 working days.

Refund and Cancellation

Any refunds will be processed in 60 days. Should there be any cancellation, it may be due to the organizer not getting the minimum participants or the participant failing to attend the workshop due to unavoidable reason.

Disclaimer

Faculty of Engineering, Multimedia University reserves the right to change the instructors, date and to vary/cancel the programme should unavoidable circumstances arise. All effort will be taken to inform participants of the changes. Upon submission of the registration form, you are deemed to have read and accepted the terms.

Enquiries

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