



VLSI Circuit Design
For
Energy Harvesting Systems

Training Programme

by

Faculty of Engineering

Multimedia University

16 – 17 December 2020

Faculty of Engineering, Multimedia University

Overview

The subject discusses VLSI system design such as number systems, switching algebra, simplification of Boolean functions, combinational logic, sequential logic, state machines including their design and implementation, timing considerations, implementation technologies, Programmable Array Logic (PALs), design methodology, CAD system, design for testability (DFT) and overview concept on energy harvesting circuits design and applications.

Objective

- To give a more enhanced view about the topics in question to the design engineers.
- To better equip the design engineers with an architectural knowledge on IC/VLSI circuit design & testability fundamental / background.
- To give overview/concept on energy harvesting circuits design.

Target Audience

VLSI system / IC design engineer.

Prerequisite

Basic knowledge of digital logic design and microelectronics.

Training Methodology

Classroom.

Course Duration

2 days.

Content/Outline

Day 1:

Hardware & software aspects of digital design:

Design entries, Design methodologies, Design flow, Design abstraction levels, Register transfer level design, Implementation platforms, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL), Complex Programmable Logic Devices (CPLD), and Field Programmable Gate Arrays (FPGA), and Computer-aided digital design tools.

Register transfers & Datapaths:

Register transfer operations, Datapaths, Micro operation, Arithmetic/logic unit, Shifter, Pipelining techniques, and Pipelined datapath.

Control unit design:

Finite state machine, Mealy model FSM, Moore model FSM, State diagram, Microcode control, and Hardwired control.

Day 2:

Testability:

Design for Testability, Test approaches: Ad-Hoc Test, Scan-Based Test, and Built-In Self-Test (BIST); Test Generation – ATPG, Fault Models - Stuck-at Fault.

Devices & Circuits for Energy Harvesting –Overview:

Energy harvesting overview, Energy autonomous systems (EAS), Energy from vibrations, Energy from light, Energy from temperature, Energy from radio-frequency, Industrial applications & some market Perspective and other applications.

Course Instructor

Name: Prof. Dr. Md. Shabiul Islam.

Dr. Md. Shabiul Islam is a Professor at the Faculty of Engineering (FOE) in Multimedia University (MMU), Cyberjaya, Selangor, Malaysia. Previously, he served (2009-2016) as an Associate Professor at The Institute of Microengineering & Nanoelectronics (IMEN) in Universiti Kebangsaan Malaysia (UKM), Bangi, Selangor, where he led Micro and Nano System Laboratory under IMEN, UKM. He served (1999-2009) as Lecturer at FOE in MMU. He served (1993-1999) as Research Assistant at the department of Electrical, Electronics &

System Engineering (EESE), UKM, Malaysia. He served (1991-1993) as a Scientific Officer at The Institute of Electronics and Material Science (IEMS) in Bangladesh Atomic Energy Commission (BAEC), Saver, Dhaka, Bangladesh.

He pursued his Ph.D. degree (2008) in VLSI design from Faculty of Engineering, MMU, Cyberjaya, Malaysia. He received his M.Sc. degree (1997) in the area of Microcontroller Based System Design from EESE, UKM, Malaysia. Previously he obtained B.Sc. (1985) and M.Sc. degree (1986) from the Department of Applied Physics & Electronics, Rajshahi University, Bangladesh. His research expertise covers a wide range of engineering disciplines. They include Micro/Nano System Design, VLSI design, Micro-powering harvesting and Microcontroller based system design, and FPGA Realization based on Fuzzy Logic (FL) Algorithm etc. He has been serving as the project leader in TM R&D (Malaysia) funded projects. He has authored more than 185 peer-reviewed publications, a few books and book chapters. He was appointed (2010-2012) as an "Associate Fellow" at EESE, UKM. Currently he has been appointed (2017-2020) as an "Associate Fellow " at IMEN, UKM.

Administrative Details

Programme Logistics

Duration: 2 days

Date: 16 – 17 December 2020

Venue: Faculty of Engineering, Multimedia University

Registration Deadline: 2 December 2020

Your Investment

Condition		Price per Pax
Regular Fee (After 11 Nov)	Students / MMU Alumni	RM700
	Public	RM1,200
	Public (Group >5 pax)	RM1,000
Early Bird Fee (Before 11 Nov)	Students / MMU Alumni	RM500
	Public	RM1,000
	Public (Group >5 pax)	N/A

Method of Payment

Please make payment via bank transfer only. Account details is as below:

Account name: Unitele Multimedia Sdn Bhd

Account number: 86-0090180-2

Bank: CIMB Islamic Bank Berhad

Payment must be made by the registration deadline.

Refund and Cancellation

Any refunds will be processed in 60 days. Should there be any cancellation, it may be due to the organizer not getting the minimum participants or the participant failing to attend the workshop due to unavoidable reason.

Disclaimer

Faculty of Engineering, Multimedia University reserves the right to change the instructors, date and to vary/cancel the programme should unavoidable circumstances arise. All effort will be taken to inform participants of the changes. Upon submission of the registration form, you are deemed to have read and accepted the terms.

Enquiries

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A horizontal banner with a green-to-teal gradient background. The text "Registration Form" is written in a bold, dark blue font, centered within the banner.

Registration Form

To register, please visit this link: <https://forms.gle/ixQ5TZHSTvzPSwzV6>